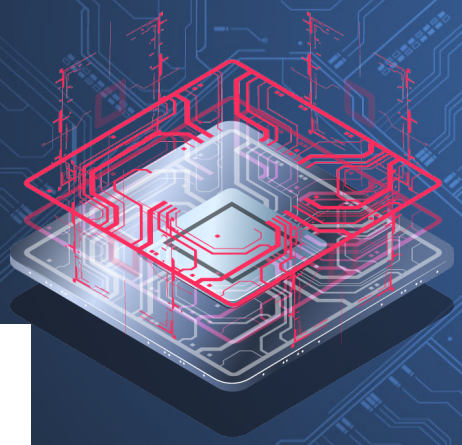
RapidSilicon

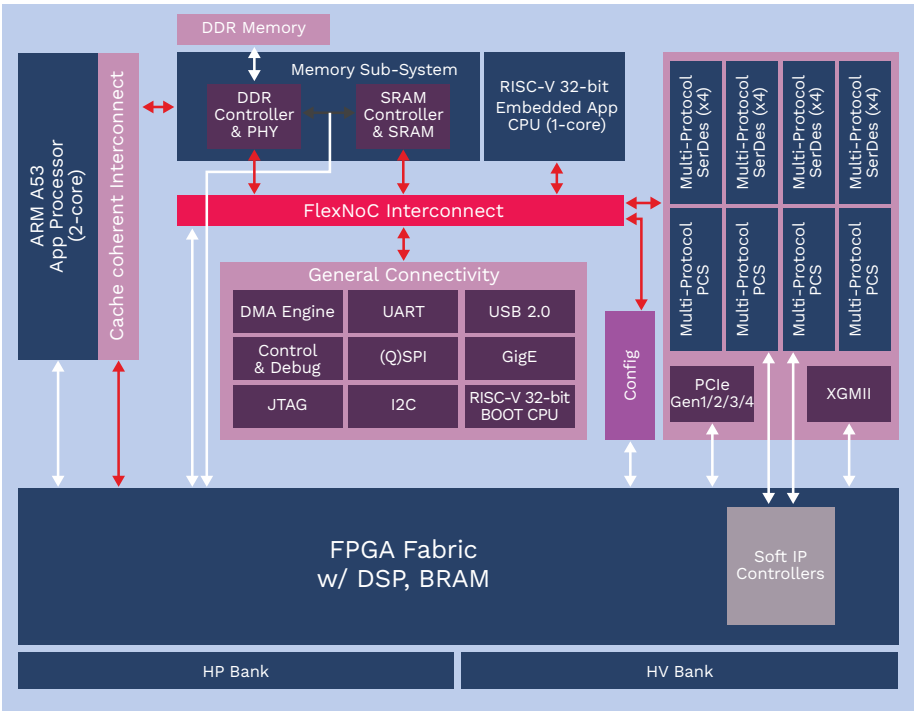


GEMINI

Optimal Performance, Power and Connectivity

The New Standard for Emerging Embedded Applications

While power, performance and cost have been the key characteristics in the embedded FPGA space for decades, integration shines bright in the new Gemini chip from Rapid Silicon. Built on TSMC's 16nm FF process, Gemini delivers the best performance-per-watt-per-dollar out of the gate. The innovative design of Gemini features proven FPGA architectures including 6-input fracturable LUTs, DSP blocks, true dual-port block RAM. This family also features hardened RISC-V, and dual-core ARM A53 processors, and includes an up to 2166 Mbps DRAM controller and 16.3125 Gbps SerDes with hard PCI Express Gen-4 and Ethernet controllers. This vast amount of IP integration is enabled via the high performance, low latency FlexNoC interconnect. The Gemini programmable logic devices bring a fresh, modern perspective and true innovation to meet the embedded markets current and future needs.



GEMINI BLOCK DIAGRAM

THE INDUSTRY GAP

FPGA usage is too diversified for a single organization to service.

Larger FPGA vendors focus on data center, communications infrastructure and higher ASP products.

Existing mid-range FPGAs do not meet current and future standards and processing needs and are approaching end of life.

RAPID SILICON FILLS THE GAP

IP and products designed from the ground up for optimal performance, power and cost.

Industry veterans and executives with combined 150+ years of experience and over 15 FPGAs and SoCs delivered successfully.

Leverage and promote the robust open source community to streamline development and support.

Bring innovation and customization to satisfy the diverse needs of the market.

RapidSilicon

A Modern PLD Using Hardened FlexNoC

Traditional PLDs have failed to meet the increasing need for IP integration in size and power-constrained embedded systems. Gemini is designed to eliminate the performance bottlenecks and interface bridging challenges with the use of hardened FlexNoC interconnect IP. Not only does this state-of-the-art IP natively support AXI, OCP, and proprietary protocol with Ncore® cache coherency, it also eliminates routing congestion, improves performance, lowers latency, reduces both die area and power consumption and provides quality of service (QoS). Gemini with hardened FlexNoC is one of the many ways Rapid Silicon has reimagined a modern, nimble FPGA that can quickly scale and adapt to the diverse and growing needs of tomorrow's embedded applications.

FABRIC ARCHITECTURE

- From 50 KLE to 250 KLE device densities
- Up to 1250 true DSP blocks on the largest device
- Up to 9.5Mb of on-chip block RAM on the largest device
- 6-input fracturable LUT with carry chain and registered outputs
- Multiply-accumulate DSP blocks with carry chain
- True dual-port 18 Kb block RAM supporting shift register and FIFO modes
- 4 output PLLs capable of generating up to 1 GHz clocking

I/O CAPABILITIES

- Highest I/O density with over 550 I/Os
- High voltage I/O supporting up to 3.3V standards
- High performance I/O capable of up to 1 GHz LVDS performance
- Lowest power and high-speed SerDes at 16.3125 Gbps

INTEGRATED IP

- Hard 32-Bit RISC-V real-time application processor with custom instruction support operating up to 533 MHz with 16 KB I/D cache and 64 KB program memory
- Hard 64-bit ARM A53 dual-core application processor with Neon and floating point unit running at 1.6 GHz
- DRAM controller capable up to 2166 Mbps performance support DDR4, DDR3 and LPDDR4
- Hardened FlexNoC interconnect allows for low latency, rapid integration of any AXI-capable IP
- Hard PCI Express controller supporting up to Gen 4 protocols
- Hard 10G Ethernet controller for easy, high performance connectivity
- Up to 512KB of dedicated on-chip RAM for extra storage